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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/717,977	MOK ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Telephone election on January 10, 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *11-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-10* is/are rejected.

7)☒ Claim(s) *2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3-15-2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to filling of the application on November 20, 2003 . Claims 1-13 are current pending, in which claims 11-13 are non-elected, without traverse.

Election/Restriction

1. Restriction to one of the following inventions is required under 35 U.S.C. § 121:

I. Claims 11-13, drawn to a multi-layer printed circuit board, classified in Class 174, subclass 255.

II. Claims 1-10, drawn to a method of manufacture thereof, classified in Class 438, subclass 629.

The inventions are distinct, each from the other because of the following reasons:

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (M.P.E.P. § 806.05(f)). Unpatentability of the group I invention would not necessarily imply unpatentability of the group II invention, since the device of the group I invention could be made by process material different than those/that of the group II invention. For example: the multilayer print circuit board can be made by not employing the release film and step of removing the release film.

Because these inventions are distinct for the reasons given above and have acquired a separate status as shown by the above different classifications and as given in the above examples, the fields of search are not co-extensive and separate examination would be required, restriction for examination purposes as indicated is proper.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

2. During a telephone conversation with Mr. Jerald Nagae on January 2005, a provisional election was made to prosecute the invention of method claims 1-10, without traverse as treated. Affirmation of this election must be made by applicant in replying to this Office action. Claims

11-13 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1,4,5,7,9 are rejected under 35 U.S.C. 102(b) as being anticipated by Applicant's admitted prior art (at present specification page 1, line 20 through page 10; Figs 1-4).

Applicant's admitted prior art teaches (at present specification page 1, line 20 through page 10; Figs 1-4) a method for manufacturing a parallel multi-layer printed circuit board, comprising the steps of: (A) forming a predetermined number of circuit layers, including the sub-steps of: (a) forming via holes 104 through a copper stack plate 102/103 (Figs 1a-1b; present specification page 4, lines 10-25); (b) plating surfaces of the copper stack plate and inner walls of the via holes with copper (Fig 1c; page 5, lines 1-20); and (c) forming circuit patterns 105 on the copper stack plate (Fig 1d; page 5, line 21 through page 6); (B) forming a predetermined number of insulating layers, including the sub-steps of: (a) forming via holes 204 through a flat-type insulating material provided with release films 202 attached to surfaces of the flat-type insulating material 203 (Figs 2a-2b,3; page 6, line 8 through page 7); (b) filling the via holes with a conductive paste 205 (Fig 2c); and (c) removing the release films 202 from the flat-type insulating material (Fig 2d); (C) alternately arranging the circuit layers and the insulating layers at predetermined positions (Fig 3); (D) pressing the arranged circuit and insulating layers (Fig 4; pages 8-9); wherein circuit patterns from the plated copper 105 are formed on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers (Figs 4,1d; page 5, line 21 through page 6). Re claims 4-5, further comprising the step of: (F) forming a target

hole at the position of a target guide mark, serving as a reference point of drilling, on the circuit layers and the insulating layers (re claim 4); and, re claim 5) wherein the sub-step (a) of each of the steps (A) and (B) includes the step of: (a') forming a guide hole at the same position, serving as a reference point of interlayer matching, on the circuit layers and the insulating layers (present specification page 8, line18 through page 9, line 11). Re claim 7, wherein the release film has a thickness of 20 to 30 microns (specification page 7, lines 1-5). Re claim 9, wherein the conductive paste 205 is considered as a point contact-type conductive paste 205 comprising metal particles (Fig 2c; specification page 7, lines 18-21).

5. Claims 1,3-5,7-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al (2004/0194303).

Kim teaches (at Figs 3A-8; paragraphs 65 through 96) a method for manufacturing a parallel multi-layer printed circuit board, comprising the steps of: (A) forming a predetermined number of circuit layers, including the sub-steps of: (a) forming via holes 304 through a copper stack plate 302/303 (Figs 3A-3B); (b) plating surfaces of the copper stack plate and inner walls of the via holes with copper 305 (Fig 1C); and (c) forming circuit patterns 306 on the copper stack plate (Fig 1d; paragraph 72; 306a-306c in Fig 7); (B) forming a predetermined number of insulating layers, including the sub-steps of: (a) forming via holes 504 through a flat-type insulating material provided with release films 502 attached to surfaces of the flat-type insulating material 503 (Figs 5A-5B); (b) filling the via holes with a conductive paste 505 (Fig 5C); and (c) removing the release films 502 the flat-type insulating material (Fig 5D; paragraphs 81-85); (C) alternately arranging the circuit layers and the insulating layers at predetermined positions (Fig 7, paragraphs 93-97); (D) pressing the arranged circuit and insulating layers (Fig 8); wherein circuit patterns 306a-306c from the plated copper 305 are formed on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers (Figs 7,8, 3d). Re claim 3, wherein surface-treatment of the copper stack plate 105 is performed so as to increase an adhering force (paragraphs 16, 21,24; Figs 1A-1E). Re claims 4-5, further comprising the step of: (F) forming a target hole at the position of a target guide mark, serving as a reference point of drilling, on the circuit layers and the insulating layers (re claim 4); and, re claim 5) wherein the sub-step (a) of each of the steps (A) and (B) includes the step of: (a') forming a guide hole at the

same position, serving as a reference point of interlayer matching, on the circuit layers and the insulating layers (paragraphs 95-96; page 7, right column, lines 7-18). Re claim 7, wherein the release film 502 a thickness of 20 to 30 microns (paragraph 82; Figs 5A-5B). Re claims 8-9, wherein the conductive paste is a metallic bond-type conductive paste 106/505 impregnated with a tin (Sn) component, or re claim 9, wherein the conductive paste is considered as a point contact-type conductive paste 106/505 (paragraphs 16,84). Re claim 10, wherein the flat-type insulating material includes a resin material in a c-stage, and resin layers in a b-stage respectively stacked on both surfaces of the resin material (paragraph 87; Figs 6A-6D,5A-5D)

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over either Kim et al (2004/0194303) or Applicant's admitted prior art (at present specification page 1, line 20 through page 10; Figs 1-4), taken with DiFranco (5,332,486).

Kim teaches (at Figs 3A-8; paragraphs 65 through 96) a method for manufacturing a parallel multi-layer printed circuit as applied to claims 1,3-5,7-10 above. Applicant's admitted prior art teaches (at present specification page 1, line 20 through page 10; Figs 1-4) a method for manufacturing a parallel multi-layer printed circuit board as applied to claims 1,4,5,7,9 above.

Kim and Applicant's admitted prior art lack mentioning buffing a portion of the conductive paste, flowing out from the via holes of the outmost layer, so as to remove the protruding portion of the conductive paste, after the step (C).

However, DiFranco teaches (at Figs 24C-25B, col 29, lines 10-22; col 28, line 58 through col 29; Figs 1A-2D; col 16, lines 46-55) to buffing a portion of the conductive paste, flowing out from the via holes of the outmost layer, so as to remove the protruding portion of the conductive paste.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to manufacture the printed circuit board of Kim or Applicant's admitted prior art by buffing a portion of the conductive paste flowing out from the via holes of the outmost layer, as taught by DiFranco. This is because of the desirability to remove the unwanted protruding portion of the conductive past flowing out form the via holes.

Allowable Subject Matter

** Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

** The following is a statement of reasons for the indication of allowable subject matter: The references of record, alone or in combination, do not anticipatively disclose each and every aspect of the claimed method, or fairly make a prima facie obvious case of the claimed method, in combination with other processing claimed limitations as recited in base claim 1, the further inclusion of claim 2 of forming, in the sub-step (c) of the step (A), a circuit pattern is formed on one surface of the copper stack plate so as to form the circuit layer arranged on an outermost layer of the printed circuit board, and circuit patterns are formed on both surfaces of the copper stack plate so as to form the circuit layer arranged on an internal layer of the printed circuit board.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-102

Michael Trinh
Primary Examiner